CLAIMS

1. An assembler of a bandwidth matching device, comprising:

a plurality of inputs, each of the plurality of inputs having a first bandwidth;

a plurality of multiplexers being equal in number to the plurality of inputs, each of the plurality of multiplexers being connected to receive the plurality of inputs and a selector signal, each of the plurality of multiplexers having a multiplexer output; and

one or more serially connected cells being connected to the multiplexer output of each of the plurality of multiplexers, the one or more serially connected cells forming a stepped arrangement of cells, the stepped arrangement of cells being defined to generate a concatenated output representing a concatenated version of one of the plurality of inputs on a cycle of a clock, the concatenated output having a second bandwidth that is larger than the first bandwidth.

2. An assembler of a bandwidth matching device as recited in claim 1, wherein each of the plurality of multiplexers is connected to receive a different selector signal in each cycle of the clock, the different selector signal being defined to control which of the plurality of inputs received by the multiplexer is to be transmitted to the multiplexer output.

3. An assembler of a bandwidth matching device as recited in claim 2, wherein the selector signal to be received by each of the plurality of multiplexers is defined by a sequence of single bit signals being equal in number to the plurality of inputs.

4. An assembler of a bandwidth matching device as recited in claim 3, further comprising:

a rotating selector for generating the single bit signals sequenced to define the selector signal, the rotating selector signal causing one of the single bit signals to have a first digital state and a remainder of the single bit signals to have a second digital state in the given clock cycle, the rotating selector causing a different one of the single bit signals to have the first digital state on successive clock cycles such that the first digital state rotates in a defined sequence among the single bit signals on successive clock cycles.

5. An assembler of a bandwidth matching device as recited in claim 1, wherein the stepped arrangement of cells is defined by decreasing a number of cells in each of the one or more serially connected cells by one cell between adjacent multiplexers.

6. An assembler of a bandwidth matching device as recited in claim 5, wherein a last cell in each of the one or more serially connected cells defining the stepped arrangement of cells is connected to provide a portion of the concatenated output on each cycle of the clock, adjacent last cells within the stepped arrangement of cells providing sequential portions of one of the plurality of inputs to adjacent portions of the concatenated output on each cycle of the clock.

7. An assembler of a bandwidth matching device as recited in claim 6, wherein a number of portions defining the concatenated output is equal to the number of the plurality of inputs.

8. An assembler of a bandwidth matching device as recited in claim 1, wherein the second bandwidth of the concatenated output is equal to the first bandwidth of each of the plurality of inputs multiplied by the number of the plurality of inputs.

9. An assembler of a bandwidth matching device as recited in claim 1, wherein each cell in the stepped arrangement of cells is a flip-flop device.

10. An assembler of a bandwidth matching device as recited in claim 1, wherein the concatenated output corresponds to a different one of the plurality of inputs on successive cycles of the clock.

11. A disassembler of a bandwidth matching device, comprising:

an input representing a concatenation of a plurality of data packets;

a plurality of cells, each of the plurality of cells being connected to receive one of the plurality of data packets, some of the plurality of cells being serially connected to a number of additional cells to form a stepped arrangement of cells, the stepped arrangement of cells being defined to provide each of the plurality of data packets in a sequenced manner; and

a plurality of multiplexers, each of the plurality of multiplexers being connected to receive the plurality of data packets provided by the stepped arrangement of cells in the sequenced manner, each of the plurality of multiplexers being further connected to receive a selector signal, each of the plurality of multiplexers being defined to provide an output sequence of data packets on successive cycles of a clock, the output sequence of data packets representing an unconcatenated sequence of the concatenation of the plurality of data packets.

12. A disassembler of a bandwidth matching device as recited in claim 11, wherein the stepped arrangement of cells is defined by increasing the number of additional cells serially connected to some of the plurality of cells by one cell between adjacent cells of the plurality of cells.

13. A disassembler of a bandwidth matching device as recited in claim 12, wherein a number of cells in the stepped arrangement of cells each provide a data packet from the plurality of data packets represented by the input to each of the plurality of multiplexers on each cycle of the clock.

14. A disassembler of a bandwidth matching device as recited in claim 11, wherein each of the plurality of multiplexers is connected to receive a different selector signal in each cycle of the clock, the different selector signal being defined to control which of the plurality of data packets received by the multiplexer is to be provided as part of the output sequence of data packets.

15. A disassembler of a bandwidth matching device as recited in claim 14, wherein the selector signal to be received by each of the plurality of multiplexers is defined by a sequence of single bit signals being equal in number to the plurality of data packets received from the stepped arrangement of cells on each cycle of the clock.

16. A disassembler of a bandwidth matching device as recited in claim 15, further comprising:

a rotating selector for generating the single bit signals sequenced to define the selector signal, the rotating selector signal causing one of the single bit signals to have a first digital state and a remainder of the single bit signals to have a second digital state in the given clock cycle, the rotating selector causing a different one of the single bit signals to have the first digital state on successive clock cycles such that the first digital state rotates in a defined sequence among the single bit signals on successive clock cycles.

17. A disassembler of a bandwidth matching device as recited in claim 11, wherein each cell in the stepped arrangement of cells is a flip-flop device.

18. A method for operating a bandwidth matching device, comprising:

receiving a number of inputs into an assembler;

transmitting the number of inputs through a stepped arrangement of cells of the assembler; and

outputting sequential portions of one of the number of inputs from the stepped arrangement of cells of the assembler to provide a concatenated output containing the sequential portions.

19. A method for operating a bandwidth matching device as recited in claim 18, further comprising:

operating a clock to produce signals for controlling the receiving of the number of inputs into the assembler, the transmitting of the number of inputs through the stepped arrangement of cells of the assembler, and the outputting of sequential portions of one of the number of inputs from the stepped arrangement of cells of the assembler.

20. A method for operating a bandwidth matching device as recited in claim 18, further comprising:

receiving a concatenated input into a disassembler, the concatenated input containing sequential portions of data;

transmitting the concatenated input through a stepped arrangement of cells of the disassembler;

outputting the sequential portions of data from the stepped arrangement of cells of the disassembler;

receiving the sequential portions of data into a number of multiplexers; and

operating the number of multiplexers to individually provide the sequential portions of data contained within the concatenated input.

21. A method for operating a bandwidth matching device as recited in claim 20, further comprising:

operating a clock to produce signals for controlling the receiving of the concatenated input into the disassembler, the transmitting of the concatenated input through the stepped arrangement of cells of the disassembler, the outputting of the sequential portions of data from the stepped arrangement of cells of the disassembler, the receiving of the sequential portions of data into the number of multiplexers, and the operating of the number of multiplexers to individually provide the sequential portions of data contained within the concatenated input.

22. A device, comprising:

a plurality of inputs, each of the plurality of inputs having a first bandwidth;

a plurality of multiplexers equal in number to the plurality of inputs, each multiplexer coupled to receive the plurality of inputs and a selector signal, each multiplexer having a respective multiplexer output; and

a plurality of cells coupled to receive the multiplexer outputs and a clock signal, the plurality of cells to generate a cell output representing a concatenated version of a different one of the plurality of inputs in relation to a cycle of the clock signal, the cell output having a second bandwidth greater than the first bandwidth, the plurality of cells including one or more cells coupled in series in a respective path from each respective multiplexer output to the cell output, a number of cells in each path differing by one from a next sequential path.

23. A device, comprising:

a multiplexing circuit to receive a plurality of input signals and a selecting signal, each input signal having a first bandwidth and the multiplexing circuit having a plurality of multiplexing output signals;

a serializing circuit coupled to receive the plurality of multiplexing output signals and a clock signal, the serializing circuit to output a serialized output signal representing a concatenated version of a different one of the plurality of input signals in relation to a cycle of the clock signal, wherein the serialized output signal has a second bandwidth; and

one or more cells coupled in series in a respective path from each of the plurality of multiplexing output signals to the serialized output signal, wherein a number of cells in each path differs by one from a next sequential path.

24. A device as recited in claim 23, wherein the multiplexing circuit includes a plurality of multiplexers equal in number to the plurality of input signals, wherein each multiplexer is coupled to receive the plurality of input signals and a selector signal, each multiplexer providing one multiplexing output signal.

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